CBT3306

Dual bus switch

Rev. 02 — 17 November 2005 Product data sheet

1. General description

The CBT3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output enable ($\overline{OE}$) input is HIGH.

The CBT3306 is characterized for operation from –40 °C to +85 °C.

2. Features

- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Package options include plastic small outline (SO) and thin shrink small outline (TSSOP)
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101

3. Quick reference data

Table 1: Quick reference data

T_{amb} = 25 °C; GND = 0 V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD}	propagation delay	from input (nA or nB) to output (nB or nA); C_L = 50 pF; V_{CC} = 5.0 V ± 0.5 V	-	-	0.25	ns
$C_{io(off)}$	off-state input/output capacitance	V_I = 3 V or 0 V; $\overline{OE}$ = V_{CC}	-	6.45	-	pF
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	-	3	µA

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
CBT3306D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
CBT3306PW	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1

PHILIPS

5. Functional diagram

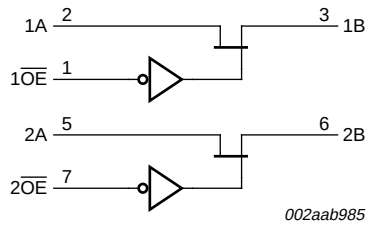


Fig 1. Logic diagram of CBT3306 (positive logic)

6. Pinning information

6.1 Pinning

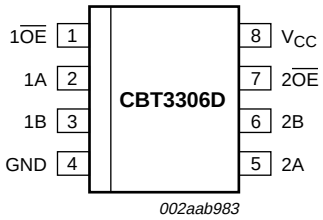


Fig 2. Pin configuration for SO8

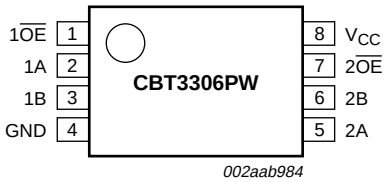


Fig 3. Pin configuration for TSSOP8

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable 1
1A	2	A port input 1
1B	3	B port output 1
GND	4	ground (0 V)
2A	5	A port input 2
2B	6	B port output 2
$2\overline{OE}$	7	output enable 2
V_{CC}	8	positive supply voltage

7. Functional description

Refer to Figure 1 “Logic diagram of CBT3306 (positive logic)”.

7.1 Function selection

Table 4: Function selection

Input	Function
$\overline{OE}$	
L	A port = B port
H	disconnect

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7.0	V
V_I	input voltage		−0.5 [2]	+7.0	V
I_O	output current		-	128	mA
I_{IK}	input clamping current	$V_{I/O}$ = 0 V	-	−50	mA
T_{stg}	storage temperature		−65	+150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Section 9 “Recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

9. Recommended operating conditions

Table 6: Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	−40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = −18 mA		-	-	−1.2	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	-	±1	µA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND		-	-	3	µA
V_{pass}	pass voltage	output HIGH; V_I = V_{CC} = 5.0 V; I_O = −100 µA		3.4	3.6	3.9	V
ΔI_{CC}	additional quiescent supply current [2]	per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND		-	-	2.5	mA
C_i	input capacitance	control pin; V_I = 3 V or 0 V		-	3.15	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; V_I = 3 V or 0 V; $\overline{OE}$ = V_{CC}		-	6.45	-	pF
R_{on}	ON-state resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA	[3]	-	3.4	5	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	[3]	-	3.4	5	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA	[3]	-	6.8	15	Ω

[1] All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two (A or B) terminals.

11. Dynamic characteristics

Table 8: Dynamic characteristics

V_{CC} = +5.0 V ± 0.5 V; T_{amb} = −40 °C to +85 °C; C_L = 50 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PD}	propagation delay	from input (nA or nB) to output (nB or nA)	[1]	-	-	0.25	ns
t_{en}	enable time [2]	from input ($n\overline{OE}$) to output (nA or nB)		1.8	-	5	ns
t_{dis}	disable time [3]	from input ($n\overline{OE}$) to output (nA or nB)		1	-	5	ns

[1] The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] Output enable time to HIGH and LOW level.

[3] Output disable time from HIGH and LOW level.

11.1 AC waveforms

V_I = GND to 3.0 V.

t_{PLZ} and t_{PHZ} are the same as t_{dis}.

t_{PZL} and t_{PZH} are the same as t_{en}.

t_{PLH} and t_{PHL} are the same as t_{PD}.

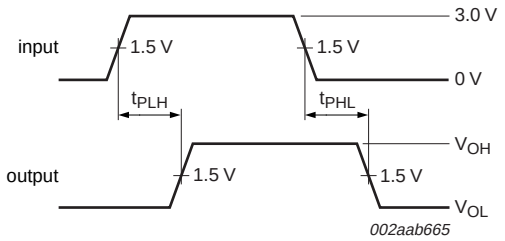
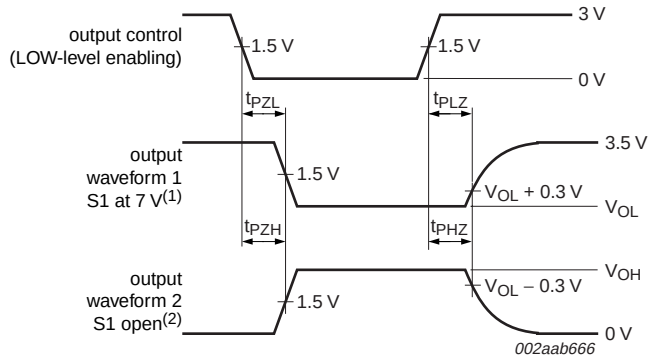


Fig 4. Input to output propagation delay

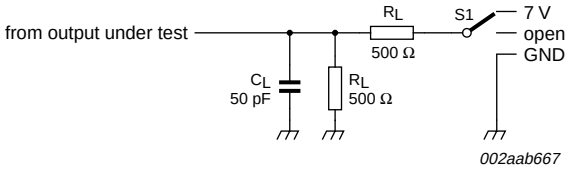


(1) Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.

(2) Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

Fig 5. 3-state output enable and disable times

12. Test information



Test data are given in Table 9.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

The outputs are measured one at a time with one transition per measurement.

C_L = load capacitance includes jig and probe capacitance.

R_L = load resistance.

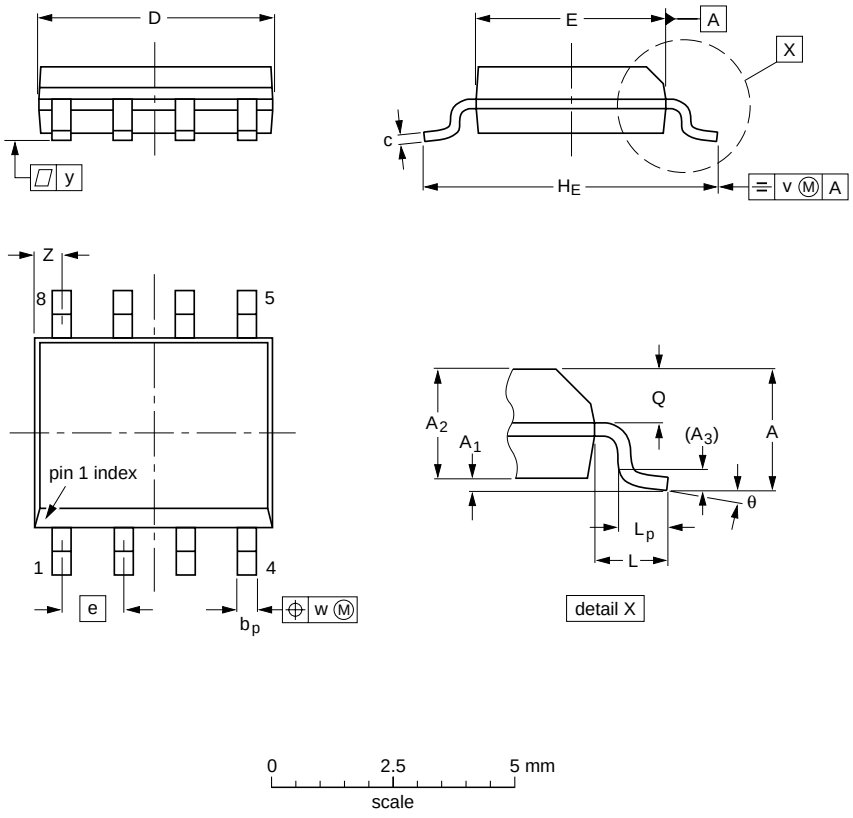
Fig 6. Test circuit

Table 9: Test data

Test	Load		Switch
	C_L	R_L	
t_{PD}	50 pF	500 Ω	open
t_{PLZ}, t_{PZL}	50 pF	500 Ω	7 V
t_{PHZ}, t_{PZH}	50 pF	500 Ω	open

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

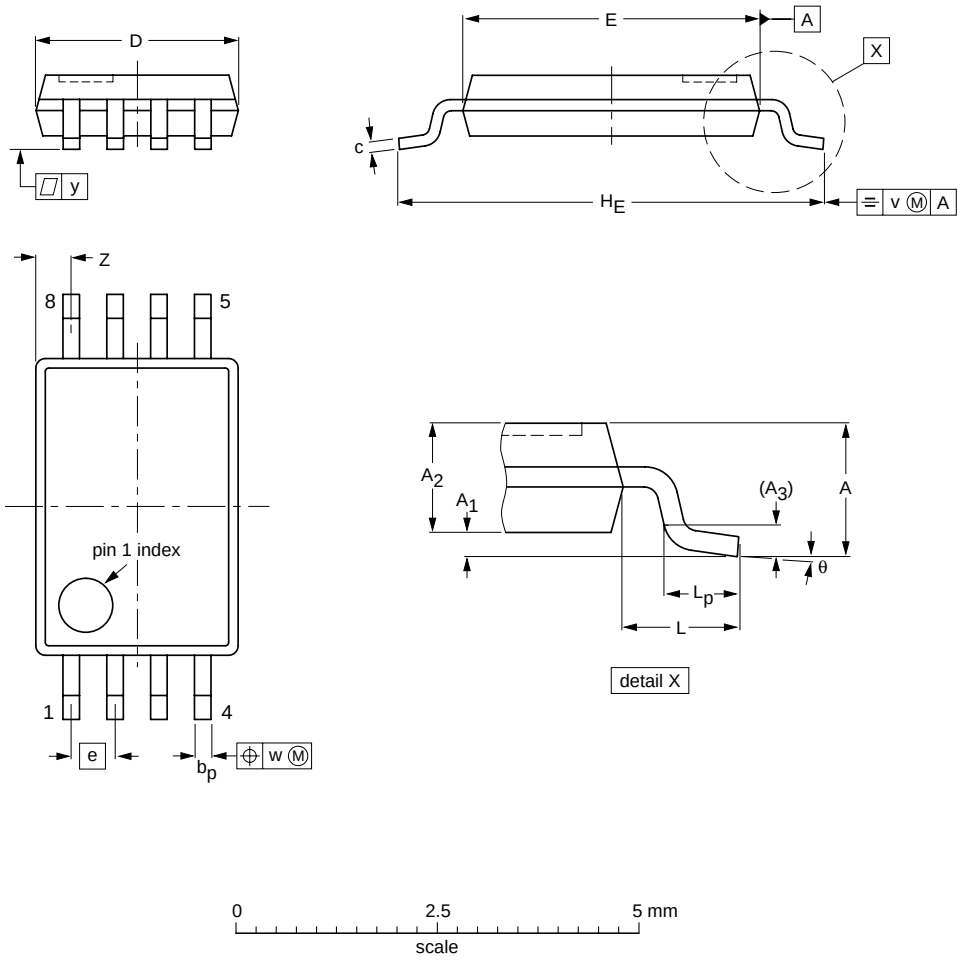
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig 8. Package outline SOT530-1 (TSSOP8)

14. Soldering

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

14.5 Package related soldering information

Table 10: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

15. Abbreviations

Table 11: Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

16. Revision history

Table 12: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
CBT3306_2	20051117	Product data sheet	-	CBT3306_2	CBT3306_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Table 1 “Quick reference data”: – added Min and Max columns; moved t_{PD} and I_{CC} values to Max column – under ‘Conditions’ for $C_{io(off)}$: changed “V_O” to “V_I” • Table 5 “Limiting values”: – changed parameter description for I_{IK} from “diode current” to “input clamping current” – deleted old table note [3] • Table 7 “Static characteristics”: – changed symbol for input leakage current from “I_I” to “I_{LI}” – under ‘Conditions’ for $C_{io(off)}$: changed “V_O” to “V_I” – R_{on} maximum value for condition V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA: changed from “7.5 Ω” to “15 Ω”				
CBT3306_1	20011108	Product data	853-2304 27313	9397 750 09115	-

17. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

18. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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22. Contents

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